REMARKS

Claims 1-17 were pending. Claims 1-3 and 15-17 are amended herein, and claims 18-20 are added herein. Claims 1-20 are pending in this application.

In an attempt to better describe the inventions, Applicant has amended claims 1-3 and 15-17, and has added new claims 18-20. Applicant believes the amended claims 1-3 and 15-17, and the new claims 18-20, are fully supported by the specification, and are in condition for allowance.

Claims 1-5 and 12-17 were rejected under 35 U.S.C. 102(e) as being anticipated by Jones (US Patent No. 6,813,753). Applicant respectfully traverses this rejection. Applicant notes that claims 1 and 14-17 are independent claims. Pending claims 2-13 and 18-19 depend from claim 1, and pending claim 20 depends from claim 15.

Jones does not teach or disclose a method for designing a circuit including multiple conductors, wherein the method includes performing a timing analysis of the circuit *at a first operating point* using conductor resistance values *modified dependent upon a determined performance difference between circuit operation at the first operating point and a second operating point*, and wherein a result of the timing analysis is *indicative of whether the circuit will operate correctly at the second operating point*. Accordingly, Jones does not disclose the limitations of independent claims 1 and 14-17.

As amended herein, claim 1 recites (emphasis added):

1. A method for designing a circuit comprising a plurality of conductors, the method comprising:

selecting a first operating point corresponding to a first circuit application;

selecting a second operating point corresponding to a second circuit application;

determining a performance difference between circuit operation at the first and second operating points;

using the performance difference to compute a factor;

applying the factor to resistance values of the conductors, thereby producing modified conductor resistance values;

performing a timing analysis of the circuit *at the first operating point using the modified conductor resistance values, thereby producing a result indicative of whether the circuit will operate correctly at the second operating point*.

Claim 14 recites "A circuit designed using the method of claim 1."

As amended herein, claims 15-17 recite (emphasis added):

15. A computer program product for designing a circuit comprising a plurality of conductors, the computer program product having a computer-readable medium with a computer program embodied thereon, the computer program product comprising:

computer program code for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values, *wherein the factor is computed dependent upon a determined performance difference between operation of the circuit at a selected first operating point, corresponding to a first circuit application, and a selected second operating point corresponding to a second circuit application*; and

computer program code for performing a timing analysis of the circuit *at the first operating point using the modified conductor resistance values, thereby producing a result indicative of whether the circuit will operate correctly at the second operating point*.

16. An apparatus for designing a circuit comprising a plurality of conductors, the apparatus comprising:

means for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values, *wherein the factor is computed dependent*

upon a determined performance difference between operation of the circuit at a selected first operating point, corresponding to a first circuit application, and a selected second operating point, corresponding to a second circuit application; and

means for performing a timing analysis of the circuit *at the first operating point using the modified conductor resistance values, thereby producing a result indicative of whether the circuit will operate correctly at the second operating point*.

17. A timing analysis system, comprising:

a memory system, comprising:

software including instructions for applying a factor to resistance values of the conductors, thereby producing modified conductor resistance values, *wherein the factor is computed dependent upon a determined performance difference between operation of the circuit at a selected first operating point, corresponding to a first circuit application, and a selected second operating point corresponding to a second circuit application*;

a timing analysis tool including instructions for performing a timing analysis of the circuit *at the first operating point using the modified conductor resistance values, thereby producing a result indicative of whether the circuit will operate correctly at the second operating point*; and

a central processing unit coupled to the memory system and configurable to fetch instructions from the memory and to execute the instructions.

Jones discloses a method for characterizing a timing delay curve of a circuit component, wherein the timing delay curve has a curvilinear region and a linear region. The method includes determining a first delay equation representing the curvilinear region, determining a second delay equation representing the linear region, and determining a corner capacitance representing a transition point from the curvilinear region to the linear region. In a method for characterizing multiple circuit components, a base component is "pre-characterized" as described above. A scaling

factor is determined, and applied to the base component to characterize the timing delay curve of another one of the circuit components.

Jones uses a circuit model (i.e., the circuit model 10 of Figure 1) to mimic the delay of a logic gate, such as a transistor, within a component (e.g., an inverter, a flip-flop, etc.). Delay refers to the time it takes for a signal to propagate from the input to the output of the logic gate or component. The model contains a resistor "R," representing the resistance of the component's output transistor, a capacitor "C," representing the component's output load, and an ideal switch "S." The resistor R is assumed to vary with time relative to an input signal "V(t)." (Jones, col. 4, lines 1-10.) Figure 2 of Jones is a graph 20 of the value of resistor R versus time relative to a change in the input signal V(t). (Jones, col. 4, lines 14-16.) After the switch S is closed (i.e., at $t = 0$), the value of the resistor R linearly decreases from a value "Rmax" to a value "Rmin" at time $t = \tau$. (Jones, col. 4, lines 29-30.) The value of the resistor R is the value Rmin for time $t \geq \tau$.

Figure 3 of Jones is a graph of delay versus load capacitance for the component modeled in Figure 1. A delay equation (i.e., an equation 7) for the time period $0 < t < \tau$ in Figure 2, during which the value of the resistor R is changing, produces a curvilinear region (i.e., a curvilinear region 31a) of the delay curve of Figure 3. Another delay equation (i.e., an equation 10) for the time period $0 < t < \tau$ in Figure 2, during which the value of the resistor R is constant and equal to Rmin, corresponds to a linear region (i.e., a linear region 31b) of the delay curve of Fig. 3. (Jones, col. 5, lines 48-53.)

While a delay model or library created using a method of Jones may be useful in performing a timing analysis of a circuit, Jones does not teach or disclose a method for designing a circuit including multiple conductors, wherein the method includes performing a timing analysis of the circuit *at a first operating point* using conductor resistance values *modified dependent upon a*

determined performance difference between circuit operation at the first operating point and a second operating point, and wherein a result of the timing analysis is *indicative of whether the circuit will operate correctly at the second operating point*.

For at least the above reasons, Applicant asserts Jones fails to teach or disclose all of the elements and limitations of pending independent claims 1 and 14-17. Applicant also believes that pending claims 2-13 and 18-19 that depend from claim 1, and pending claim 20 that depends from claim 15, are also allowable for at least the above reasons.

Claims 6-11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of Publication No. 2004/0025136 to Carelli, Jr. ("Carelli"). Applicant respectfully traverses this rejection. Applicant notes that pending claims 2-13 and 18-19 depend from claim 1 reproduced above.

The combination of Jones and Carelli does not teach or disclose a method for designing a circuit including multiple conductors, wherein the method includes performing a timing analysis of the circuit *at a first operating point* using conductor resistance values *modified dependent upon a determined performance difference between circuit operation at the first operating point and a second operating point*, and wherein a result of the timing analysis is *indicative of whether the circuit will operate correctly at the second operating point*. Accordingly, the combination of Jones and Carelli does not disclose the limitations of independent claim 1 and claims 2-13 and 18-19 that depend from claim 1.

As described above, Jones discloses a method for characterizing a timing delay curve of a circuit component, and a method for characterizing the timing delay curves of multiple circuit components by scaling of a base component.

Carelli discloses a method of generating a new technology library (see Carelli Figure 2) at a selected or desired temperature/voltage (T/V) point. A set of at least three temperature/voltage (T/V) points are pre-characterized for a given technology library. A two-dimensional space is created in which temperature is plotted against supply voltage. An interpolation method is used to generate the new technology library at the selected T/V point within the two-dimensional space. (Carelli, pg. 2, para. [0015].)

While a delay model or library created using a method of Jones and/or Carelli may be useful in performing a timing analysis of a circuit, the combination of Jones and Carelli does not teach or disclose a method for designing a circuit including multiple conductors, wherein the method includes performing a timing analysis of the circuit *at a first operating point* using conductor resistance values *modified dependent upon a determined performance difference between circuit operation at the first operating point and a second operating point*, and wherein a result of the timing analysis is *indicative of whether the circuit will operate correctly at the second operating point*.

For at least the above reasons, Applicant asserts the combination of Jones and Carelli fails to teach or disclose all of the elements and limitations of pending independent claim 1. Applicant also believes that pending claims 2-13 and 18-19 that depend from claim 1 are also allowable for at least the above reasons.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-20 are in condition for allowance, and respectfully request allowance of pending claims 1-20.

With the amendments to the claims presented herein, there are currently 5 pending independent claims and 20 total pending claims in the application. As the original application had 5 independent claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 10/19/05

CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003

Gregory W. Carr
Reg. No. 31,093

Amendments To The Drawings

No amendments have been made to the drawings.